ASSIGNMENT 7

Textbook Assignment: "Computer Memories," chapter 6—continued, pages 6-20 through 6-32, and "Input/Output (I/O) and Interfacing," chapter 7, pages 7-1 through 7-20.

7-1. Semiconductor memories are known by all of the following terms except which one?

1. Read/write memory
2. Scratch-pad memory
3. Random access memory
4. Read-only memory

7-2. Semiconductor memories have which of the following characteristics?

1. Destructive readout and volatile
2. Destructive readout and nonvolatile
3. Non-destructive readout and volatile
4. Non-destructive readout and nonvolatile

7-3. Each RAM chip contains which of the following items?

1. One memory cell only
2. One memory cell and the logic to support it only
3. Large numbers of memory cells only
4. Large numbers of memory cells and the logic to support them

7-4. On RAM chips, memory cells are organized based on which of the following factors?

1. Number of memory words only
2. Number of bits per word only
3. Number of memory words and number of bits per word
4. Number of gate arrays

7-5. The transistors used in flip-flops of static RAM may be MOS or bipolar. Compared to MOS, bipolar has what advantage, if any?

1. Higher density
2. Higher access speed
3. Requires less space
4. None, they both have the same advantages

7-6. In a static RAM, the address lines are used to enable the addressed memory cell flip-flop circuit by row and column number.

1. True
2. False

IN ANSWERING QUESTION 7-7, REFER TO FIGURE 6-31 ON PAGE 6-24 OF THE TRAMAN.

7-7. Data is stored, or read from, the memory cells of SRAM via a total of how many lines?

1. One
2. Two
3. Three
4. Four

7-8. The (a) address lines and the (b) I/O data lines are usually tied to what buses?

1. (a) Computer or memory system bus
   (b) Computer or memory system bus
2. (a) Computer or memory system bus
   (b) Data bus
3. (a) Data bus
   (b) Computer or memory system bus
4. (a) Data bus
   (b) Data bus

7-9. During a SRAM read cycle, what is (a) the status of the write enable and (b) the mode of the data buffers?

1. (a) True (b) input
2. (a) True (b) output
3. (a) False (b) input
4. (a) False (b) output

IN ANSWERING QUESTION 7-10, REFER TO FIGURE 6-32 ON PAGE 6-25 OF THE TRAMAN.

7-10. Each dynamic RAM cell consists of which of the following devices?

1. One MOS transistor only
2. One tiny capacitor only
3. One MOS transistor and one tiny capacitor only
4. Many MOS transistors and several tiny capacitors

7-11. DRAM cells do not retain their charged state for more than a few milliseconds. This degradation is due to which of the following factors?

1. Time only
2. Temperature only
3. Time and temperature
4. Temperature and power

7-12. To retain their charged state, DRAMs must be refreshed. Of the following methods, which one is (a) more cost effective because it uses what (b) device?

1. (a) Internal
   (b) Battery backup
2. (a) Internal
   (b) Single refresh address generator
3. (a) External
   (b) Battery backup
4. (a) External
   (b) Single refresh address generator

7-13. In DRAM organization, the data input and data output lines may be tied together in what type of application, if any?

1. One that uses a unidirectional data bus
2. One that uses a bidirectional data bus
3. None, they are never tied together

7-14. Compared to a SRAM, a DRAM has all except which of the following advantages?

1. It retains its charged state
2. It has lower power consumption
3. It has higher density
4. It is less complex

7-15. Programs stored on ROM are often referred to as firmware for which of the following reasons?

1. They are software only
2. They are hardware only
3. They are more hardware than software
4. They write data into the ROM address

7-16. Compared to RAM, ROM has all of the same operational characteristics except which of the following?

1. Allows random access
2. Uses a row/column arrangement
3. Can be read by normal computer accessing methods
4. Can be written to by normal computer accessing methods

7-17. ROM has what primary use?

1. Stores data addresses for recovery purposes
2. Allows the computer to perform I/O operations
3. Provides a user interface through a panel
4. Stores the content of the computer registers for interrupt processing

7-18. The acronym BIOS stands for what term?

1. Basic input/output system
2. Bipolar input/output status
3. Binary input/output status
4. Bidirectional input/output system

7-19. The acronym NDRO stands for what term?

1. Non-destructive readover
2. Non-destructive readout
3. Non-dynamic readover
4. Non-dynamic readout

IN ANSWERING QUESTION 7-20, REFER TO FIGURE 6-35 ON PAGE 6-28 OF THE TRAMAN.

7-20. In the example, the ROM chip memory array has a total of(a) how many decoders and (b) how many lines are input to these decoders?

1. (a) 2 (b) 12
2. (a) 2 (b) 13
3. (a) 4 (b) 12
4. (a) 4 (b) 13

7-21. ROMs may be made of which of the following materials?

1. Hardwired and magnetic only
2. Fusible links only
3. MOS and bipolar transistors only
4. Hardwired, magnetic, fusible links, and MOS and bipolar transistors

7-22. To perform ROM operations, which of the following circuits are used?

1. Timing and control signals only
2. Registers, flip-flops, and internal buses only
3. Internal buses, timing, and control signals only
4. Timing, control signals, registers, flip-flops, and internal buses

7-23. Compared to PROM, an erasable PROM has what additional advantage, if any?

1. It can be used over and over again without reprogramming
2. It can be erased and reprogrammed
3. It can be field programmed by an authorized technician
4. None, there is no additional advantage

7-24. While still in the circuit, which of the following PROMS can (a) be programmed and (b) erased?

1. (a) EAPROM/EEPROM
   (b) EAPROM/EEPROM
2. (a) EAPROM/EEPROM
   (b) UV EPROM
3. (a) UV EPROM
   (b) EAPROM/EEPROM
4. (a) UV PROM
   (b) UV PROM

7-25. A device that serves as a shared entry point from a local-area network into a larger information resource is which of the following?

1. Gateway
2. Input/output adapter (IOA)
3. Input/output controller (IOC)
4. Data terminal equipment (DTE)

7-26. A function that transfers status by using the appropriate control signals from a transmitting device to the receiving computer is which of the following?

1. Input data (ID)
2. Output data (OD)
3. External fiction (EF)
4. External interrupt (EI)

7-27. The I/O processor controls which of the following transfers?

1. The transfer of data between registers
2. The transfer of information between main memory and the CPU
3. The transfer of timing signals between the ALU and the CPU
4. The transfer of information between main memory and the external equipments

7-28. Establishing, directing, and monitoring transfers with external equipments are the functions of which of the following devices?

1. CPU
2. IOA
3. IOC
4. Bidirectional bus

7-29. Changes to input and output control and data signal voltages are functions of which of the following devices?

1. CPU
2. IOA
3. IOC
4. Bidirectional bus

7-30. The type of connectors for the I/O channels or ports will be dictated by which of the following factors?

1. Interfacing
2. Serial I/O
3. Parallel I/O
4. Voltage levels

7-31. The driver circuits are used for which of the following tasks?

1. To pass data to the IOC
2. To seticlear output registers
3. To pass interface signals to the IOC
4. To pass interface and data signals to the external equipments

7-32. External microcomputer I/O operations are usually handled by which of the following devices?

1. A single serial port
2. A single parallel port
3. A single printed circuit board
4. Multiple printed circuit boards

7-33. Examples of consistencies found in the architecture of a computer's I/O section include which of the following?

1. Types of external equipments
2. The arrangement and format of the information exchanged
3. The type and number of interfaces possible
4. The type of circuits used to process I/O information

7-34. If a printer senses a paper jam during a print operation, which of the following actions would occur?

1. A control word would be sent by the computer specifying an error condition
2. A control word would be sent to the computer specifying an error condition
3. A data word would be sent by the computer specifying a special condition
4. A data word would be sent to the computer specifying a special condition

7-35. Handshaking is also known by which of the following terms?

1. Function control word
2. External interrupt words
3. Both 1 and 2 above
4. Alphabetic and numeric data exchange

7-36. The type of interface used when all bits of information represented by a byte or word are input or output simultaneously is known as which of the following formats?

1. Serial format
2. Parallel format
3. 8-bit word format
4. 32-bit word format

7-37. Command instructions provide control over which of the following areas/operations?

1. Main memory
2. CPU operations
3. IOC single and dual channel operations
4. Interrupt driven I/O operations

7-38. The I/O command start instruction accomplishes which of the following actions?

1. Specifies an IOC, then halts further CPU processing
2. References specific main memory addresses
3. Executes a previously stored IOC command
4. Indicates to the CPU that the command has been processed

7-39. The CPU will delay processing while waiting for an I/O operation only during which of the following actions?

1. Execution of input chain operations
2. Execution of output chain operations
3. Actual data transfer operations
4. Executions of an I/O command start instruction

7-40. The actual execution of chaining instructions is independent of the CPU.

1. True
2. False

7-41. Input and output chains deal primarily with which of the following activities?

1. The processing of IOC control words
2. Specification of the locations of external status words
3. Transfer of blocks of information
4. Addresses provided by the load control memory command

7-42. Data transfer between the computer and external equipments will take place when which of the following conditions is/are met?

1. The memory areas for the data have been specified by the computer programs
2. The external equipment is ready to send or receive data and has sent a request signal
3. Initiate input/output or equivalent instruction is executed by the CPU
4. All of the above

7-43. Which of the following is one of the constants in all I/O operations?

1. Data words will always be limited to 16 bits
2. When the data transfer will begin
3. The circuitry required to connect external equipments
4. A serial data interface between the computer and external equipments

7-44. In I/O operations, communications with the external equipment require which of the following devices/operating modes?

1. An IOC
2. A single channel operating mode
3. Circuitry that specifies a sequence of events
4. A dual channel operating mode

7-45. When an index address in main memory is specified by an external equipment during an I/O operation, the computer is operating in which of the following modes?

1. Intercomputer channel mode
2. Externally specified index mode
3. Externally specified address mode
4. Dual channel mode

7-46. In I/O operations, which of the following is one of the primary uses of registers?

1. To enable and route data information only
2. To enable and route control information only
3. To enable and route both control and data information
4. To provide timing circuitry for I/O interfacing

7-47. Decoder circuits are used for which of the following purposes?

1. Main timing
2. I/O processors
3. Address translation
4. Data buffers

7-48. Status registers are used for which of the following purposes?

1. To enable and route data using the internal bus system
2. To hold or buffer data during interchanges between the very fast CPU and slower external equipments
3. To hold control data generated by main memory or the CPU when operating with very fast external equipments
4. To hold information for the CPU that indicates the operating condition and current activities of the external equipments

7-49. In computers with an IOC, once started the master clock can be stopped when which of the following actions occurs?

1. Computer master clear
2. External interrupt
3. Input data request
4. Output data request

7-50. In computers with an IOC, the master clock is started when which of the following actions occurs?

1. The computer is initially powered on
2. The computer is auto restarted
3. Both 1 and 2 above
4. An execute master clear is issued

7-51. The I/O control circuits are controlled by which of the following means?

1. The CPU
2. The IOC
3. The I/O master clock
4. The computer program

7-52. A sequential set of memory locations that contains data to be sent out or an area that is set aside for data to be received is called which of the following?

1. An input register
2. An output register
3. Both 1 and 2 above
4. A buffer

7-53. Which of the following are unbuffered operations?

1. Data transferred between computer and external devices
2. Where data is exchanged between the
3. CPU and various parts of the computer
   Both 1 and 2 above
4. Data exchanged between external devices offline

7-54. The I/O processor's sequencing circuits control which of the following actions?

1. The order in which events will be executed based upon the translated function code
2. The order in which memory addresses of data to be retrieved or stored will be acted on
3. The order in which external equipment output requests will be acknowledged
4. The order in which external interrupts will be acted on by the computer

7-55. The CPU interfaces with the I/O processor through which of the following means?

1. Special interface circuits
2. The CPU's I/O instructions
3. The sequencing circuitry
4. The maintenance console

7-56. I/O control memory words are set aside in main memory to control which of the following actions?

1. Data transfers for I/O buffer functions
2. The sequence of I/O operations
3. Parallel operations
4. Serial operations

7-57. In parallel operations, each I/O channel has its own block of memory addresses for which of the following operations?

1. Input and output only
2. External function only
3. External interrupt operations only
4. Input, output, external function, and external interrupt operations

7-58. Serial operations are affected by which of the following factors?

1. Character size, parity selection, and asynchronous interfacing only
2. Parity selection, baud rate, and synchronous interfacing only
3. Character size, parity selection, and synchronous and asynchronous interfacing only
4. Character size, parity selection, baud rate, and synchronous and asynchronous interfacing

7-59. Monitor words are used for which of the following purposes?

1. To monitor external equipment status
2. To monitor bytes that are to be transferred by the pending operation
3. To store characters for comparison with received data characters
4. To monitor main memory for the next available address for chaining instructions

7-60. Another term for accumulator based I/O is which of the following?

1. Direct CPU interface
2. Direct memory access
3. Interrupt driven I/O
4. Memory mapped I/O

7-61. The CPU handles all I/O transactions by executing one or more instructions for each word of information transferred. This process is known by which of the following terms?

1. Polled I/O
2. Memory mapped I/O
3. Interrupt driven I/O
4. Accumulator based I/O

7-62. In memory mapped I/O, the CPU accesses the I/O device by which of the following means?

1. Tieing peripheral devices directly into the communication bus
2. Placing appropriate addressing information on the bus
3. Checking each channel or port to determine if it has data for input or is ready to accept output data
4. Using an I/O processor for interface between memory and the external equipments

7-63. During direct CPU interface operations, the CPU continuously tests the status register. This technique is known by which of the following terms?

1. Memory mapped I/O
2. Accumulator based I/O
3. Interrupt driven I/O
4. Polled I/O

7-64. The main advantage of direct memory access is which of the following?

1. Speed
2. Reliability
3. Less complicated circuity
4. Maximum utilization of memory

7-65. When the CPU and the DMA attempt to access main memory simultaneously, the CPU has priority.

1. True
2. False

7-66. When a high speed disk drive is used, output data will be in which of the following forms?

1. Octal
2. Binary
3. Octal coded decimal
4. Various; form is dependent on type of interface used

7-67. The technique used when more than one peripheral device is connected to a single port/channel is known by which of the following terms?

1. Daisy chaining
2. Independent request control
3. External interrupt control method
4. Request/acknowledge control method

7-68. When more than one peripheral device is connected to a single port/channel, the priority of a device is determined by which of the following factors?

1. The CPU
2. The I/O controller
3. The computer program
4. The order of connection

7-69. When using a request and acknowledge system, the priority of the fictions and channels is determined by which of the following factors?

1. The CPU
2. The I/O controller
3. The computer program
4. The order of connection

7-70. Communication formats are governed by which of the following items?

1. The type of external equipment
2. The speed of the external equipment
3. The interfacing standard
4. The speed of the computer

7-71. The compatibility of voltage levels between the computer and external equipments is ensured by which of the following means?

1. The CPU
2. The I/O processor
3. The I/O interfacing components
4. The type and number of pins in the cable connectors

7-72. Transfer of data within a digital computer is accomplished internally using which of the following means?

1. Standard I/O interfaces
2. Serial format
3. Parallel format
4. Serial interface board

7-73. The conversion of data for transmission over a serial channel is accomplished by which of the following means?

1. A serial interface board
2. A standard format interface
3. A universal receiver-transmitter
4. I/O control printed circuit board

7-74. When a universal synchronous-asynchronous receiver transmitter is used, it functions as which of the following devices?

1. A microprocessor
2. An I/O serial interface board
3. An I/O parallel interface board
4. A peripheral device to the microprocessor

7-75. The universal synchronous-asynchronous receiver transmitter's specific asynchronous interfacing is controlled by which of the following means?

1. The bidirectional tristate data bus
2. The I/O control printed circuit board
3. The read/write control logic
4. The CPU